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Corrections of Hardware Manual

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MB90495

hm90495-cm44-10114-3e-x1-01

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Addendum, MB90495G Hardware Manual (hm90495-cm44-10114-3e)

This is the Addendum for the Hardware Manual hm90495-cm44-10114-3e of the MB90495G microcontroller series. It describes all known discrepancies of the MB90495G microcontroller series Hardware Manual.

Ref. Number (Internal ref. number) (Text Link)	Date dd.mm.yy	Version No.	Chapter/Page	Description/Correction
HWM90495001	16.09.02	1.00		Behaviour of MB90V495 and MB90F497
HWM90495002		1.00	9.3	Watch Timer, incorrect values in Figure 9.3-1
HWM90495003		1.00	15	UART, description of multi-master mode corrected
HWM90495004		1.00	12	16-Bit I/O Timer, typo in Pre-scaler settings
HWM90495005		1.00		Power-on Port behaviour
HWM90495006		1.00	22	Setting a mode, wrong memory size mentioned
HWM90495007		1.00	21	CAN, 'Hit and Away' description added
HWM90495008		1.00		Serial Flash Programming
HWM90495009		1.00	21.2	Interrupts, A/DC and EIIOS usage
HWM90495010		1.00	21.2	Interrupts, ICU and EIIOS usage
HWM90495011	03.12.02	1.01		Transition to standby mode, Standby Cancel failure behavior added

Following behaviour of MB90V495 and MB90F497, fixed with MB90V495G and MB90F497G series.

1. UART 0/1 clock

If clock input output SCK0/SCK1 is used, some conflicts may occur. This problem will be fixed with MB90V495G and MB90F497G version.

2. CAN Interface

Under very certain circumstances, it possibly may happen that the CPU reads wrong data from the CAN-RAM if the CAN Macro itself has access to the CAN RAM as well. This may lead to wrong CAN data reception or CPU register corruption. This problem will be fixed in MB90V495G and MB90F497G version.

HWM90495002

Chapter 9. Watch Timer

Chapter 9.3.1 Watch Timer Control Register (WTC)

Incorrect values in Figure 9.3-1, see correction below

			Interval time
WTC2	WTC1	WTC0	Sub osc. 32.768KHz
0	0	0	31.25ms
0	0	1	62.5ms
0	1	0	125ms
0	1	1	250ms
1	0	0	500ms
1	0	1	1s
1	1	0	2s
1	1	1	4s

Chapter 15 UART1:

15.1 Overview of UART1

In the description : ... (Multiprocessor mode) is only available for the master system.

Chapter 7.1 Overview of 16-bit Input/Output Timer

Old:

● Functions of 16-bit free-run timer

- Count clock is selected from four machine clock division ratios. The external clock signal input to the16-bit free-run timer clock input pin (FRCK) can also be used as a count clock.

Should be replaced with:

● Functions of 16-bit free-run timer

- Count clock is selected from eight machine clock division ratios. The external clock signal input to the16-bit free-run timer clock input pin (FRCK) can also be used as a count clock.

   Internal clock: ϕ, $\phi/2$, $\phi/4$, $\phi/8$, $\phi/16$, $\phi/32$, $\phi/64$, $\phi/128$

Power On : Port behaviour

Affected devices	Corrected at version/date code
MB90V495	
MB90V495G	
MB90F497	
MB90F497G	MB90F497G, 0218-Z24

Description:
When the external reset, RSTX, is not asserted during Power On, pins on port 0 and 1 will be in an undefined state. Pins on port 2, 3, 4, 5 and 6 enter High-Z upon Power on reset.

To make sure that all ports are High-Z, the external reset RSTX must be kept asserted for the entire power on reset period.

If the external reset gets disasserted during the power on reset period, the pins on port 0 and 1 will become undefined.

Output "unknown value", when the power supply is turned on If F^2MC-16LX is used.

Note:
  Output "unknown value" of pin 00 to pin 7 and pin 10 to pin 17 port, when the power supply Is turned on.

(**Single chip, Internal ROM external bus):**
  Pin 00 to pin 07 and pin 10 to pin 17 terminal become "unknown value" (output "H", "L" level or output "Hi-z") under "power-on reset" (stabilized times (2 * oscillation clock frequency) of clamping circuit for internal power supply), when the power supply is turned on, and when "power-on reset" function operates and RSTX terminal is "H" level.
If you want to output "Hi-z" under "power-on reset", it is applied reset input " "L" level " from external and so pin 00 to pin 07 and pin 10 to pin 17 terminal become "Hi-z" condition during the time.
Note:
    This workaround will work for Mode pin setting 011 (Single chip, Internal ROM external bus), 110 (Burn_In ROM), 111 (EPROM mode)
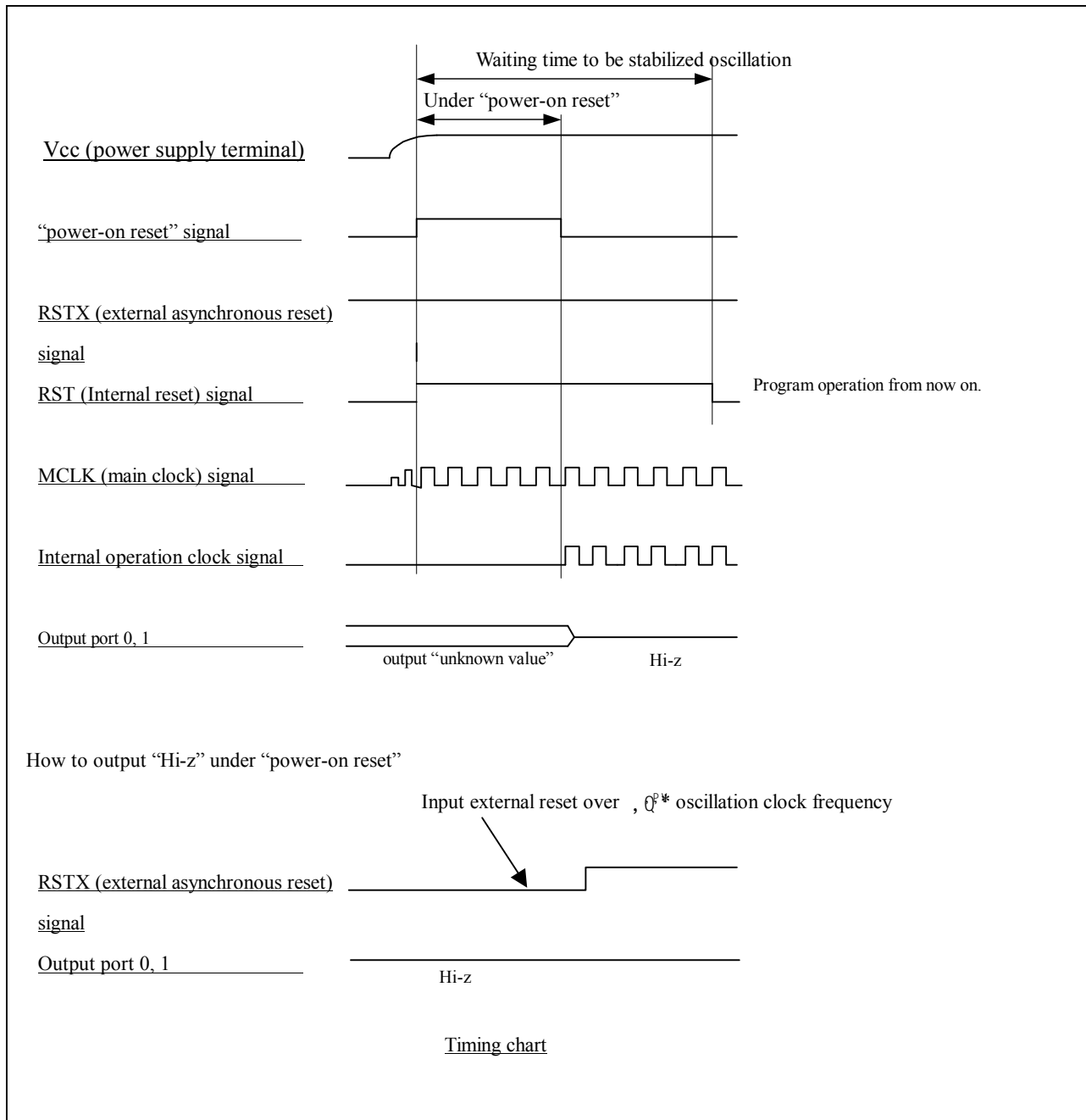
  It shows timing chart in detail the next page.

(**External Rom mode):**
Pin 00 to pin 07 and pin 10 to pin 17 terminal become "unknown value" (output "H", "L" level or output "Hi-z") under "power-on reset" (stabilized times (2 * oscillation clock frequency) of clamping circuit for internal power supply), when the power supply is turned on, and when "power-on reset" function operates and RSTX terminal is "H" level.
If you want to output "Hi-z" under "power-on reset", it is applied reset input " "L" level " from external and so pin 00 to pin 07 and pin 10 to pin 17 terminal become "Hi-z" condition during the time.

Following Ports will drive a Level: P30='L' and P31='H' and cannot be set to High-Z by asserting RST.

Waiting time to be stabilized oscillation

Under "power-on reset"

Vcc (power supply terminal)

"power-on reset" signal

RSTX (external asynchronous reset) signal

RST (Internal reset) signal

Program operation from now on.

MCLK (main clock) signal

Internal operation clock signal

Output port 0, 1

output "unknown value"

Hi-z

How to output "Hi-z" under "power-on reset"

Input external reset over , 0^p * oscillation clock frequency

RSTX (external asynchronous reset) signal

Output port 0, 1

Hi-z

Timing chart

Under "power-on reset" 2^{17} * oscillation clock frequency
(8.192ms in case of oscillation clock frequency = 16MHz)

Waiting time to be stabilized oscillation 2^{17} * oscillation clock frequency
(16.384ms in case of oscillation clock frequency = 16MHz)

Chapter 3.1 Memory Space

Chapter 3.1.1 Mapping of and Access to Memory Space

Figure 3.1-2: Memory Map for MB90495G Series

wrong address for lower external bus area mentioned.

old:

003800h

001100h

New:

003800h

002000h

Chapter 16 CAN

'Hit and Away' description:

Affected Parts: MB90V495/G, MB90497/G, MB90F497/G

Caution for disabling Message Buffers by BVAL bits

1 Caution for Reception

<u>1.1 Behaviour</u>

If there is a complete (no error until 6th bit of EOF) incoming message that have passed the acceptance filter, then this message is stored into a message buffer x (with x=0…15). If this store operation coincides with reset operation of the corresponding BVAL bit (BVALx=0), the received message will be stored into the message buffer 0 regardless of register settings. Note that this coincidence has to happen within a specific CAN-clock cycle (see event 2 in figures). Hence, the probability is very low.
If transmission request of buffer 0 is set (TREQ0=1), the above-mentioned behaviour will lead to the following transmission of a message. This message consists of the received ID, DLC and Data together with original IDE and RTR bits set of the message buffer 0.
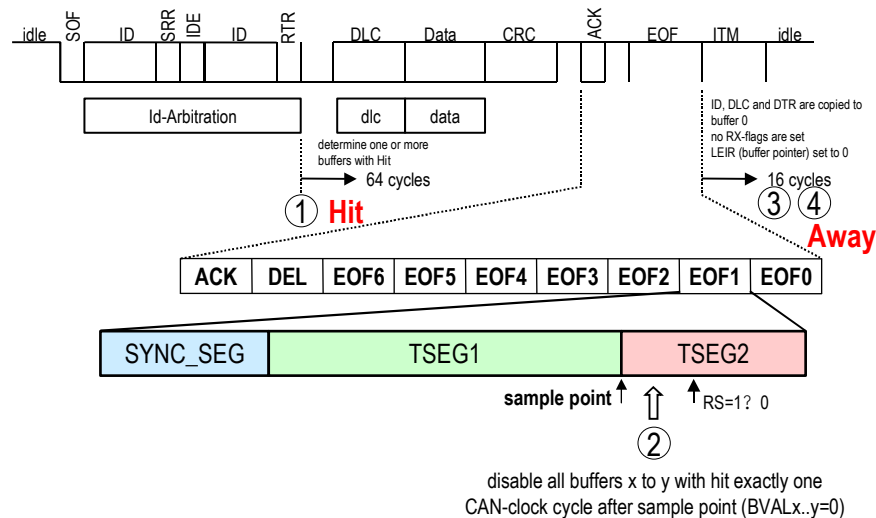However, if there are two or more message buffers with passing acceptance filers for the incoming message and only buffer x is disabled, the message will be stored into the 2nd prioritised message buffer.

If there are two or more message buffers with passing acceptance filers for the incoming message and all those buffers are disabled, the message will be stored into buffer 0.

1.2 Operation to avoid

When disabling message buffers by the BVAL register, it must be avoided that the write operation to the BVAL register coincides with the store operation of the received message in the CAN Controller.
The following diagram illustrates the timing to be avoided for the BVAL write operation.

①   CAN-controller determines buffers, which can store the message, because their acceptance filters had been passed.
②   Software disable all buffers with hit exactly one CAN-clock cycle after the sample point of EOF1.
③   CAN-controller stores received ID, DLC and data in buffer 0 regardless of the buffers determined in ①.
④   CAN-Controller sets LEIR to point to buffer 0 but RX-flags (RCR, ROVR, RRTRR) are not set.
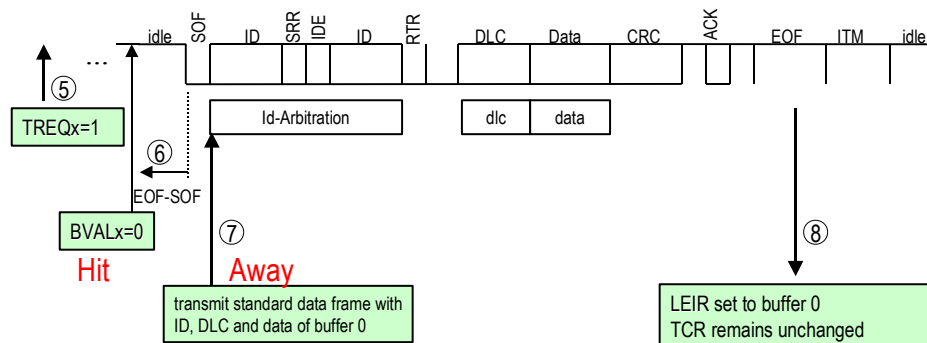④

2. Caution for Transmission

2.1 Behaviour

When there is a pending transmission of buffer x and the CAN bus status is in Intermission or in Bus Idle, the CAN-controller will load the message from buffer x in order to send it. If this load operation coincides with disabling the pending message buffer x by clearing the BVAL bit, this results in transmission of a Standard message. This message consists of RTR=0, IDE=0, DLC, 11 ID bits and Data stored in the message buffer 0.
Note that this coincidence has to happen with in a specific CAN-clock cycle. Hence, the probability is very low. The position of that cycle depends also on previous frame reception and occurrence of error frames.

2.2 Operation to avoid

When disabling message buffers by the BVAL register, it must be avoided that the write operation to the BVAL register coincides with the preparation for the next transmission in the CAN Controller.
The following diagram illustrates the timing to be avoided for the BVAL write operation.

⑤   Software requests transmission of buffer x by setting TREQx.
⑥   Software disables the buffer x by clearing BVALx.
⑦   CAN-controller transmits a standard data frame with ID, length code and data of buffer 0.
⑧   After completion of frame only LEIR is updated for buffer 0. However, TCR is not set (neither for buffer 0 nor for buffer x).

3. Correct Operation

3.1 Operation for re-configuring receive message buffers

Depending on CAN applications, it may be necessary to re-configure message buffers after receiving messages through the already active CAN communication. While the CAN bus is active, it is necessary to follow one of the two operations described below to re-configure message buffers by ID, AMS and AMR0/1 register settings. "Active" means that read value of the HALT bit is 0 and the CAN Controller is ready to receive and transmit messages.

1.1.1 Use of HALT bit
Write 1 to the HALT bit and read it back for checking the result is 1. Then change settings for the ID/AMS/AMR0/1 registers.

1.1.2 No use of Message Buffer 0
Do not use the message buffer 0. In other words, disable message buffer (BVAL=0), prohibit receive interrupt (RIE=0) and do not request transmission (TREQ=0).

3.2 Operation for processing received message.

When reading a received message from a message buffer, consideration must be given for possible over-write operation by next incoming messages. Disabling receive operation by the BVAL bit must not be used for this purpose. Use the ROVR bit for checking, if over-writing has been performed. For details, refer to description of ROVR in the hardware manual.

3.3 Cancellation of transmission request

Do not use the BVAL bit for suppressing/cancellation of transmission request. The TCANR bit is prepared for this purpose.

3.4 Composing transmission message

When composing a transmission message by writing to ID, data and other registers, the message buffer should be disabled by the BVAL bit.
In this case, the BVAL bit should reset (BVAL=0) after checking if the TREQ bit is 0 or after completion of the previous message transmission (TC=1).

4. Example of avoiding Hit-And-Away

1. Do not use message buffer 0. Keep it always disabled (BVAL0 = 0). By not using buffer 0 the processing of wrongly received messages in buffer 0 is avoided. Even if data are received in this buffer, they have no influence.
2. Set an unused 11-Bit identifier in buffer 0. "Unused" means that the identifier has no meaning to any node in the network. If an invalid standard data frame is sent according to the condition described in "0
2. Caution for Transmission", that frame must not cause misoperation of other nodes.
3. Use overrun test while processing a received message. After temporarily saving received message, test for overrun (ROVRR). If overrun occurred, read the buffer again, because the read data before overrun could be inconsistent.
4. Wait for completion of transmission. A buffer must not be disabled by clearing the BVAL-flag, as long as there is a pending transmission. Easiest way to wait for transmission completion is to use transmission interrupt but polling of TREQ is also possible.

HWM90495008

Serial Flash Programming not possible

Affected devices	Corrected at version/date code
MB90F497, 9948	MB90F497, 0003 MB90F497G not affected

Description:
It is not possible the use the serial Flash Programming mode (mode pin settings: MD2=1, MD1=1, MD0=0). Programming the Flash must be done via parallel Programmer.

HWM90495009

Chapter 3.5 Interrupts

3.5.1 Interrupt Factor and Interrupt Vector

 Interrupt Factor, Interrupt Vector, and Interrupt Control Register

Affected devices	Corrected at version/date code
MB90F497, 9948	MB90F497, 0003 MB90F497G not affected

Description:
It is not possible to use EIIOS with A/D Converter.

Workaround: Use normal Interrupt for affected date codes.

HWM90495010

Chapter 3.5 Interrupts

3.5.1 Interrupt Factor and Interrupt Vector

 Interrupt Factor, Interrupt Vector, and Interrupt Control Register

Affected devices	Corrected at version/date code
MB90F497, 9948	MB90F497, 0003 MB90F497G not affected

Description:
It is not possible to use EIIOS with Input Captures.

Workaround: Use normal Interrupt for affected date codes.

Transition to standby mode

The definition of Standby Cancel Failure is that the CPU will execute wrong
instructions when an interrupt is executed during transition to Standby mode
*0 at a certain time. Fujitsu can reproduce this phenomenon Fujitsu internally
and has found the cause.

*0:Definition of Standby mode
Main sleep mode, PLL sleep mode, Sub-sleep mode
Time base timer mode, Watch mode, Main watch mode
Main stop mode, PLL stop mode, Sub-stop mode
*Main watch mode is only for MB90370 series.

In the following cases, no problem occurs:
-Standby mode is not used
-Standby mode is released only by external reset

For further information refer to 'F2MC16-LX Standby Cancel Failure' document.