



# **MB90495 Series**

## **Draftversion 1.5**

Ó Application Microcontroller  
Fujitsu Microelectronics Europe GmbH  
Am Siebenstein 6-10  
63303 Dreieich-Buchschlag / Germany

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Vers. 1.0

Addendum and Corrections of the Hardware Manual HM90495-draftv1-5

### **1. UART 0/1 clock**

If clock input output SCK0/SCK1 is used, some conflicts may occur. This problem will be fixed with MB90V495G and MB90F497G version.

### **2. CAN Interface**

Under very certain circumstances, it possibly may happen that the CPU reads wrong data from the CAN-RAM if the CAN Macro itself has access to the CAN RAM as well. This may lead to wrong CAN data reception or CPU register corruption. This problem will be fixed in MB90V495G and MB90F497G version.

**The following entries contains all known errors of the Hardware Manual of MB90495 series.**

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Table 11.1-1+11.2-1 Watch Timer Interval Selection (Page 252+253)

			Interval time
WTC2	WTC1	WTC0	Sub osc. 32768KHz
0	0	0	31.25ms
0	0	1	62.5ms
0	1	0	125ms
0	1	1	250ms
1	0	0	500ms
1	0	1	1s
1	1	0	2s

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Chapter12: 16-Bit I/O Timer

in chapter 12.2 Register page 256

TCCSH upper 8bits of TCCS register.

TCCS (16bit) address: 58H

TCCSL (lower 8bit of TCCS) address: 58H

TCCSH:

Address 59H	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit09	Bit08
name	FRCK	--	--	--	--	--	--	--
Default value	0	--	--	--	--	--	--	--

**Bit description:**

Bit15 FRCK: defines whether to use external Clock or Internal clock for the 16 Bit I/O Timer

Bit value	description
0	internal clock used (default)
1	external clock used

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Chapter 13.4 .1 Timer Control status register, high part ( TMCSR0, TMCSR1: H)

The CSL1, CSL0 settings are incorrect. See correction below:

CSL1	CSL0	Clock Source (Machine cycle $\Phi=16\text{MHz}$ )
0	0	$\Phi/2^1$ (0.125 $\mu\text{s}$ )
0	1	$\Phi/2^3$ (0.5 $\mu\text{s}$ )
1	0	$\Phi/2^5$ (2.0 $\mu\text{s}$ )
1	1	External event count mode

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