



Technical Data

CC750

The CC750 serial communications controller is a highly integrated device that performs serial communication according to the CAN protocol. It performs all serial communication functions such as transmission and reception of messages, message filtering, transmit search, and interrupt search with minimal interaction from the host microcontroller, or CPU.

The CC750 supports the standard and extended message frames in CAN Specification 2.0 Part A and Part B. It has the capability to transmit, receive, and perform message filtering on extended message frames.

The CC750 features a serial interface (SPI) to connect a CPU without spending many interconnections.

The CC750 provides storage for 15 message objects of 8-byte data length. Each message object can be configured as either transmit or receive except for the last message object. The last message object is a receive-only buffer with a special mask design to allow select groups of different message identifiers to be received.

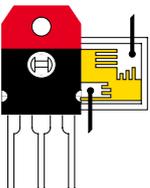
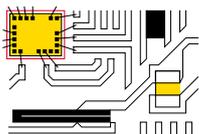
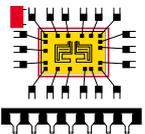
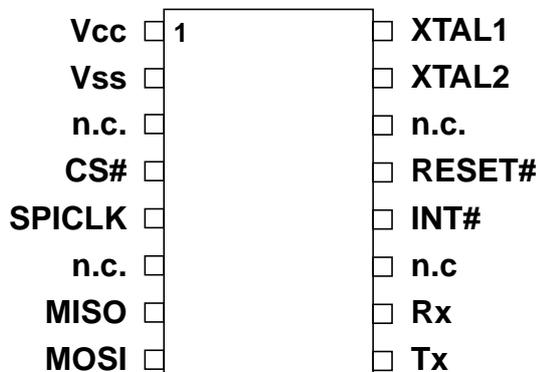
The CC750 also implements a global masking feature for message filtering. This feature allows the user to globally mask any identifier bits of the incoming message. The programmable global mask can be used for both standard and extended messages.

The CC750 is available in a SOIC16-W package. It is designed for the automotive temperature range (-40 C to +125 C).

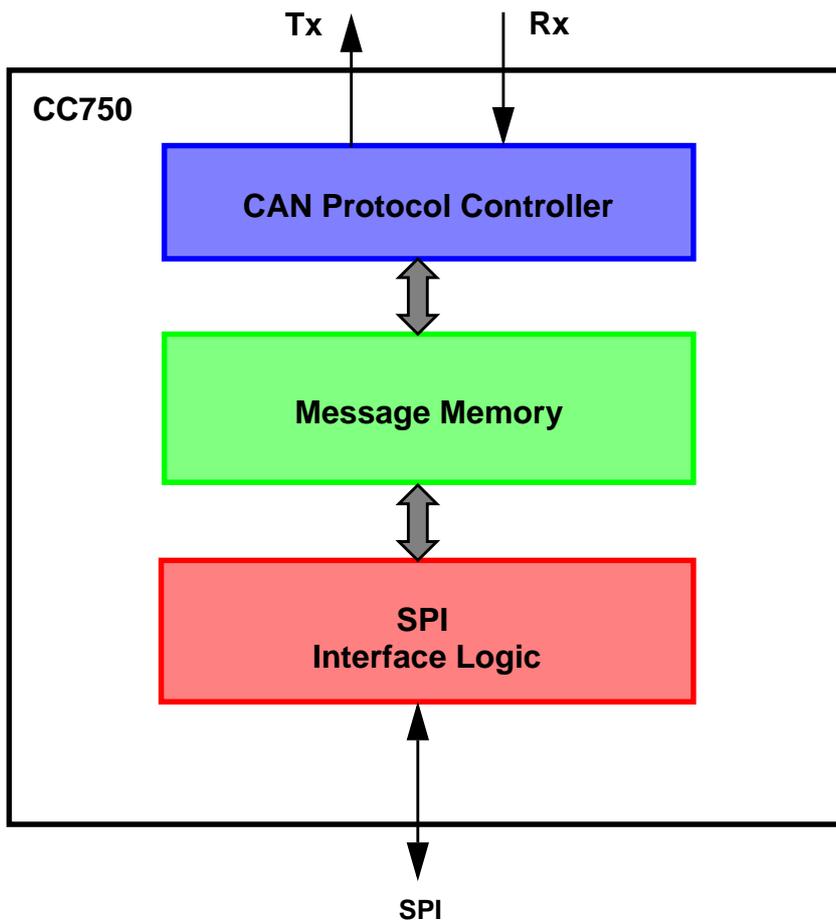
FEATURES

- Supports CAN Protocol Version 2.0 Part A, B
- Programmable Bit Rate
- 15 Message Objects of 8-Byte Data Length (14 Tx/Rx Buffers / 1 Rx Buffer)
- Programmable Global Mask (Standard and Extended Message Identifier)
- Serial Interface
- SOIC16-W Package

PINOUT



BLOCK DIAGRAM



CAN-Protocol Controller

The CAN controller controls the data stream between the Memory (parallel data) and the CAN busline (serial data). The CAN controller also handles the error management logic and the message objects.

Message Memory

Stores Message Objects and Identifier Masks and contains Rx/Tx Shift Register.

Interface Logic

The CPU Interface Logic controls the data stream between the SPI (serial data) and the Memory (parallel data).