

Active Errata List

- CAN – Sporadic Errors
- PCA – Incorrect Behavior with CPU X2 Mode Bit of HSB
- Timer0/1 – Extra Interrupt

Errata History

Lot Number	Errata List
all lots from A02543	1, 2, 3

Errata Description

1. CAN – Sporadic Errors

When BRP = 0 or when BRP > 0 and SMP = 0, the CAN controller may desynchronize and send one error frame to ask for the retransmission of the incoming frame, even though it had no error.

This is likely to occur with BRP = 0 or after long inter frame periods without synchronization (low bus load). The CAN macro can still properly synchronize on frames following the error.

Workaround

Setting BRP greater than 0 in CANBT1 and SMP equals 1 in CANBT3 allows re-synchronization with the majority vote, and thus fixes the issue.

The sampling point might have to be slightly advanced for the majority vote to take place within the bit. Therefore, at maximum speed of 1Mbit/s, the sampling point should be at less than 80% (e.g. 75%) for XTAL = 16 MHz or less than 85% (e.g. 80%) for XTAL = 20 MHz.

2. PCA – Incorrect Behavior with CPU X2 Mode Bit of HSB

When starting the microcontroller in X2 mode upon reset with the X2 fuse bit of the HSB, the PCA may not work properly when configured with Timer0 in X1 mode as clock input.

Workaround

Set the CPU in X2 mode by software by writing CKCON register at the begin of the application.

3. Timer0/1 – Extra Interrupt

When Timer0 is in X1 mode and Timer1 in X2 mode and vice versa, extra interrupt may randomly occur for Timer0 or Timer1.

Workaround

Use the same mode for the two timers.



CAN Microcontrollers

AT89C51CC03

Errata Sheet





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